REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended claim 1 so as to further clarify the intended subject matter of the present disclosure. Claims 1-3 and 7 were also amended to address the objections thereto and rejection under 35 U.S.C. § 112, second paragraph. Applicants appreciate the Examiner's suggestion for overcoming the § 112 rejection, which has been adopted. No new matter has been added.

For at least the reasons set forth below, it is respectfully submitted that the pending claims are patentable over the cited prior art.

II. The Rejection Of The Claims Under 35 U.S.C. § 102

Claims 1, 3, 7 and 8 were rejected under 35 U.S.C. § 102 as being anticipated by USP Pub. No. 2001/0043085 to Shimazaki and by USP No. 6,489,828 to Wang. For at least the following reasons, it is respectfully submitted that claim 1, as amended, is not anticipated by either of the cited prior art references.

Claim 1 relates to a level shift circuit and recites in pertinent part that "a drain of the first N-channel transistor is directly connected to a drain of the first P-channel transistor and a gate of the second P-channel transistor, [and] a drain of the second N-channel transistor is directly connected to a drain of the second P-channel transistor and a gate of the first P-channel transistor."

For example, referring to the exemplary embodiment of Fig. 1, as is shown therein, the drain of the first N-channel transistor Tn1 is **directly** connected to the drain of the first P-channel transistor Tp1, and the drain of the second N-channel transistor Tn2 is **directly** connected to the

drain of the second P-channel transistor Tp2.

Turning to the pending rejection and the cited prior art reference, it is asserted that transistors MP11 and MP10 of Shimazaki correspond to the recited first and second P-channel transistors, and that transistors MN15 and MN14 correspond to the recited first and second N-channel transistors. However, as shown in Fig. 12 of Shimazaki, the drain of the first N-channel transistor MN15 is connected to the drain of the first P-channel transistor MP11 through the N-channel transistor MN11, and the drain of the second N-channel transistor MN14 is connected to the drain of the second P-channel transistor MP14 through the N-channel transistor MN10. Thus, at a minimum, Shimazaki does not disclose or suggest a device in which the drain of the first N-channel transistor Tn1 is **directly** connected to the drain of the first P-channel transistor Tp1, and the drain of the second N-channel transistor Tn2 is **directly** connected to the drain of the second P-channel transistor Tp2 as recited by amended claim 1.

It is further noted that in accordance with the device recited by claim 1, when the level shift is operated, for example, when the second P-channel transistor Tp2 and the first N-channel transistor Tn1 turn ON, a current flows through a resistor connected between the transistors Tp2 and Tn1. This resistor in the given embodiment is transistor Tp3, which is constantly in the ON state.

In contrast, according to the device of Shimazaki, the N-channel transistor MN10 is in the OFF state during the level shift operation. Therefore, a current does not flow from the second P-channel transistor MP10 to the first N-channel transistor MN15 through the N-channel transistor MN17 that is normally in the ON state. The N-channel transistor MN17 that is normally in the ON state is provided to work during the non-operation of the level shift as described in paragraph [0105] of Shimazaki.

Thus, for at least the foregoing reasons, it is clear that Shimazaki fails to disclose or suggest the foregoing element recited by amended claim 1.

Turning to Wang, as shown in Fig. 3, Wang discloses that the transistor MN4 is controlled by the XNOR gate 264 to be in the OFF state during the operation of the level shift (*see,* col. 9, lines 31-39 and Table 3 of Wang). Thus, the transistor MN4 of Wang does NOT serve as a resistor during the operation of the level shift. As such, transistor MN4 cannot be properly deemed to correspond to the recited resistance element (e.g., transistor Tp3) of claim 1. In contrast to the recited resistance element, the transistor MN4 of Wang is controlled by the XNOR gate 264 so as to be in the ON state during an abnormal operation (see, col. 9, lines 54-60 of Wang). Accordingly, Wang also fails to disclose or suggest all of the elements recited by pending claim 1 for at least the foregoing reasons.

Accordingly, as it is well known that anticipation under 35 U.S.C. § 102 requires that each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference, *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed Cir. 1987), and that the elements must be arranged as required by the claim, *In re Bond*, 910 F. 2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990), and both Shimazaki and Wang fail to do so for at least the reasons set forth above, it is clear that neither Shimazaki nor Wang anticipate claim 1.

III. Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.,*

819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as the pending independent claim is patentable for at least the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable.

IV. Summary

Applicant submits that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

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Respectfully submitted,

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